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Packet-Level Static Timing Analysis for NoCs

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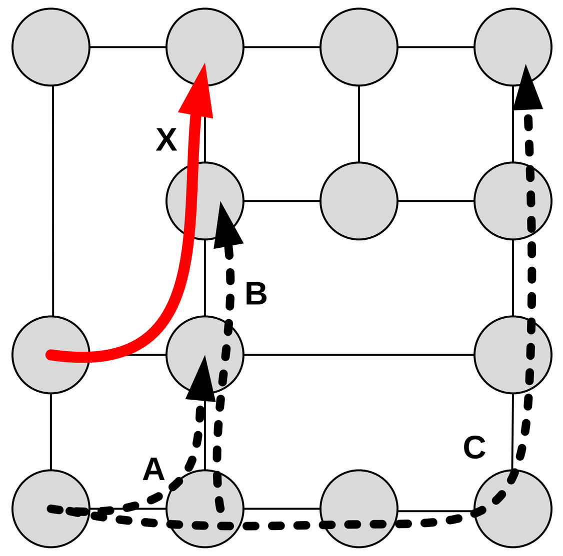
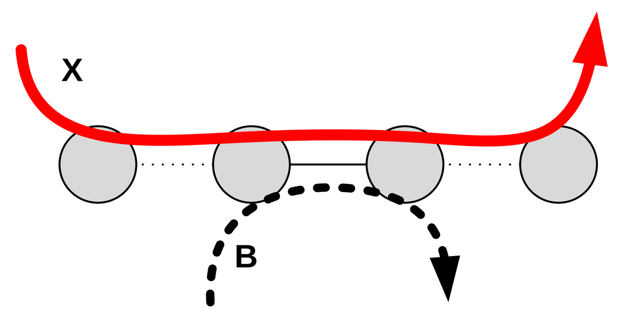
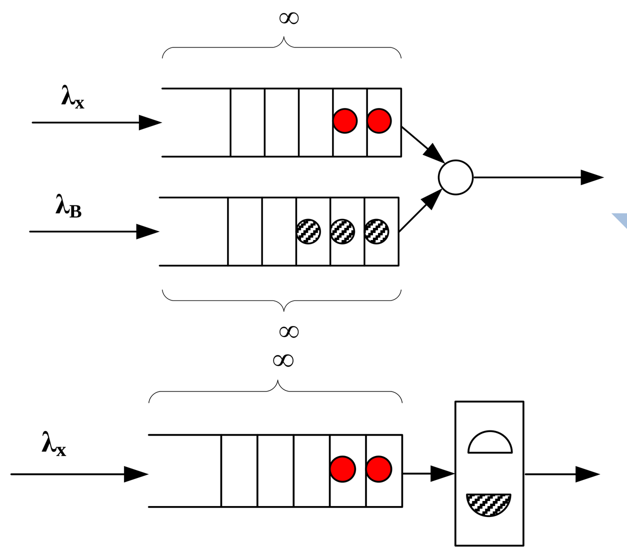
We present a methodology for packet-level static timing analysis in NoCs. Our methodology enables quick and accurate gauging of the performance parameters of a virtual-channel wormhole NoC without using simulation techniques and supports any topology, link capacities, and buffer depths. It provides per-flow analysis that is orders-of-magnitude faster than simulation while being both significantly more accurate and more complete than prior static modeling techniques. Our methodology is inspired by models of industrial flow-lines. Use of the model in a placement optimization problem is shown as an example application of the method.



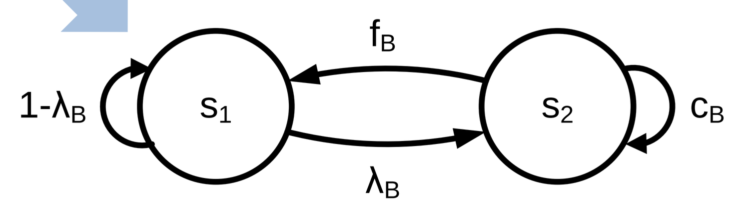
We focus on the NoC service for a particular flow of interest, which we generically call *flow X.*

The behavior of *flow X* is represented by the following queues and flow line diagrams.





Markov chain is used to express flow line's state.



$$c_\alpha = 1 - f_\alpha$$

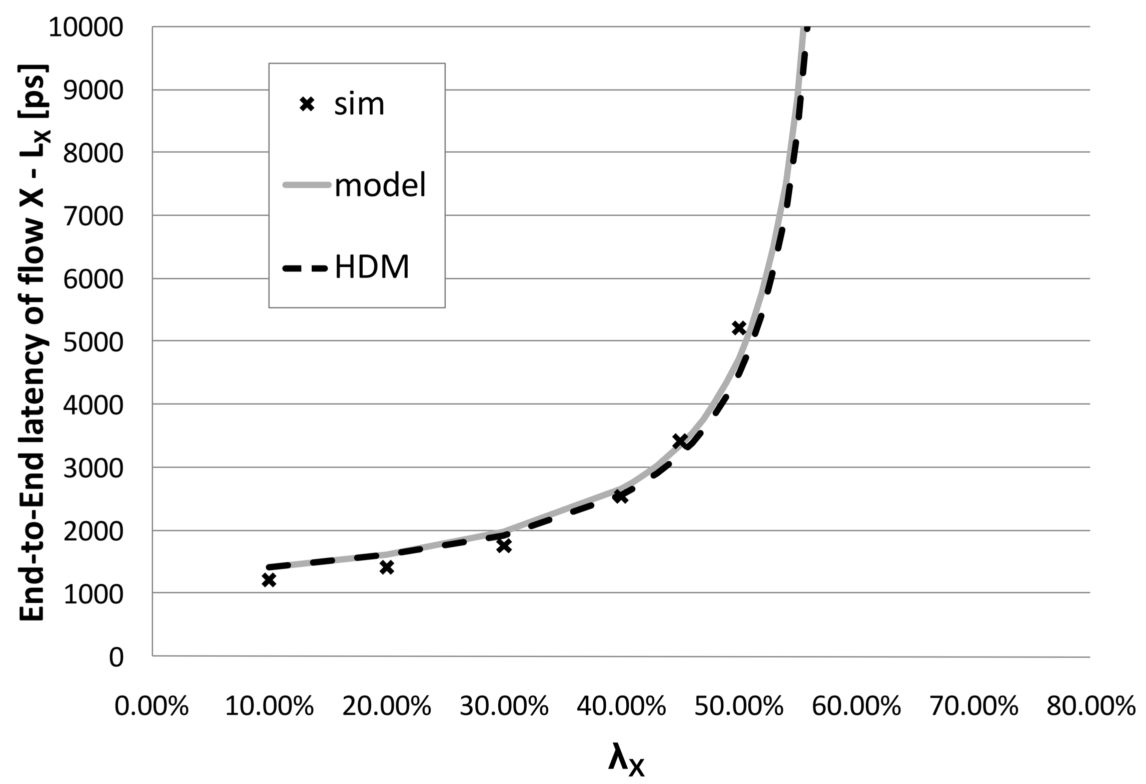
$$f_\alpha = \max\left(\frac{\phi}{2M_\alpha} - \lambda_\alpha, 0\right)$$

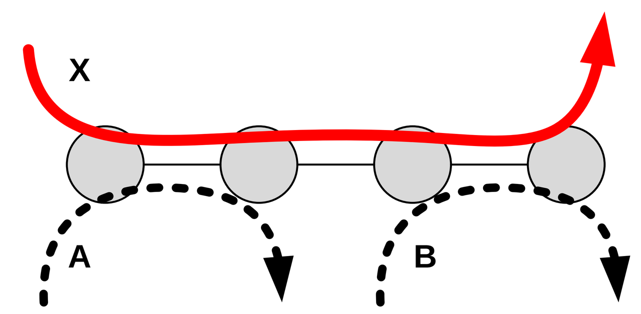
$$L_x \approx W_x + \frac{1}{T_x}$$

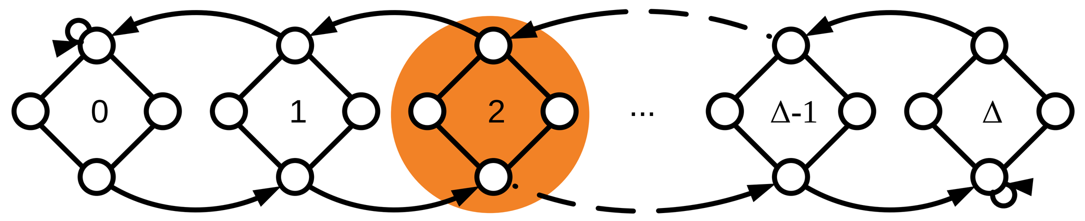
$$W_x = \frac{\left(1 + C_{S_x}^2\right)\lambda_x}{2T_x\left(T_x - \lambda_x\right)}$$

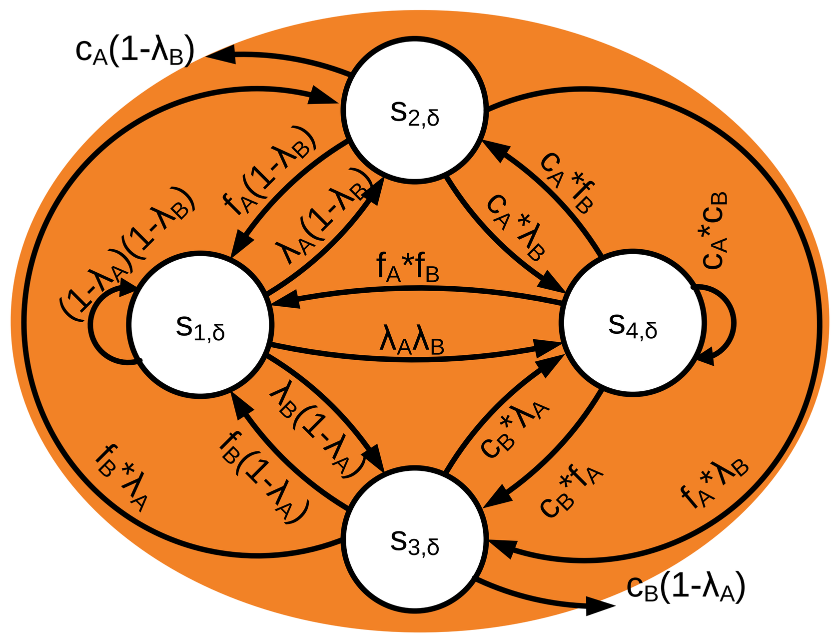
$$T_x = \sum \pi_i \rho_i$$

End-to-end latency derived using the ergodic property of the Markov chain and M/G/1 model.

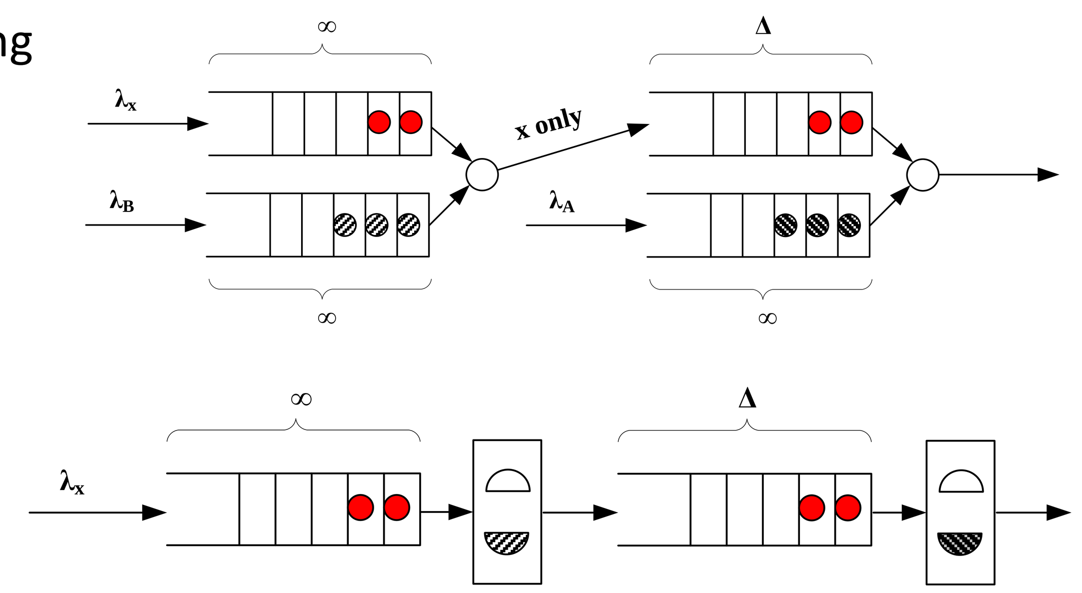


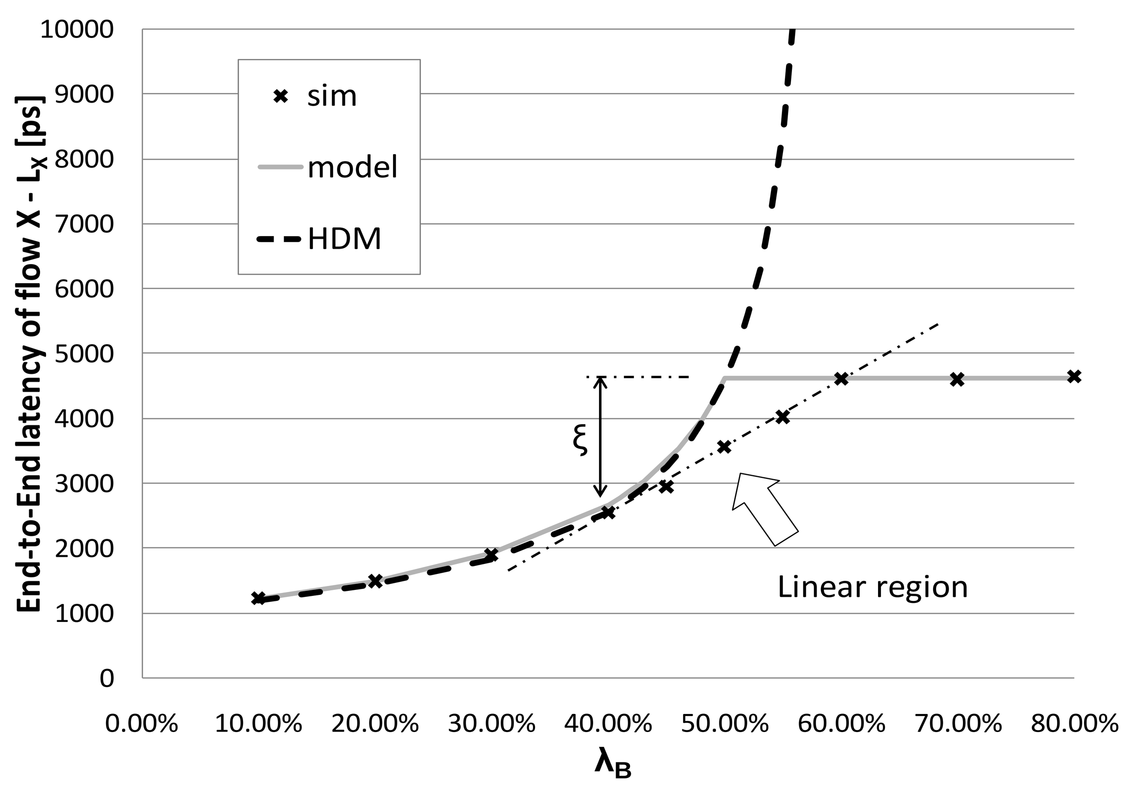


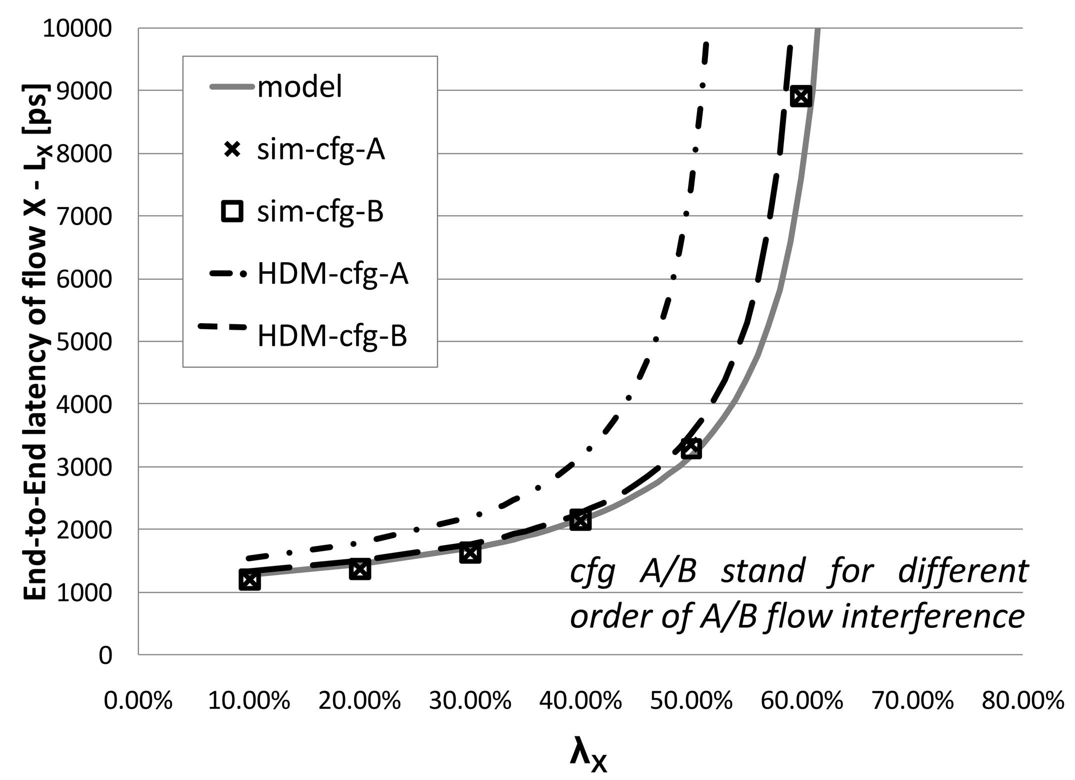


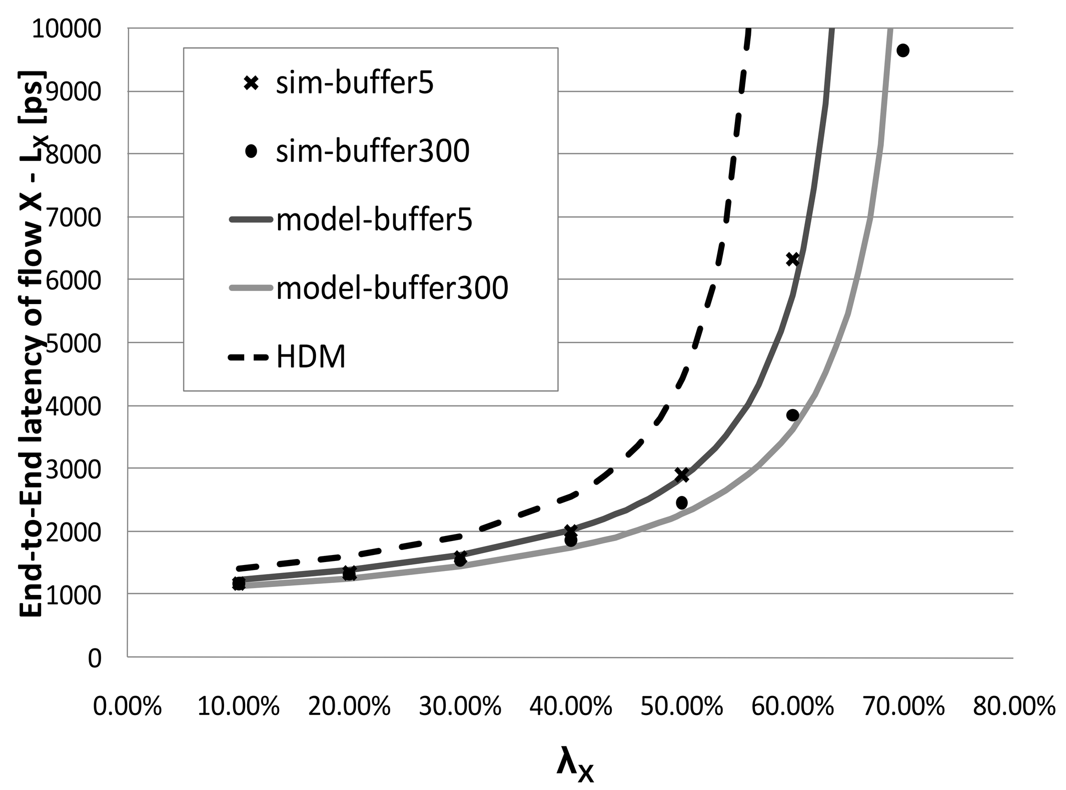


Tandem interfering flows example:

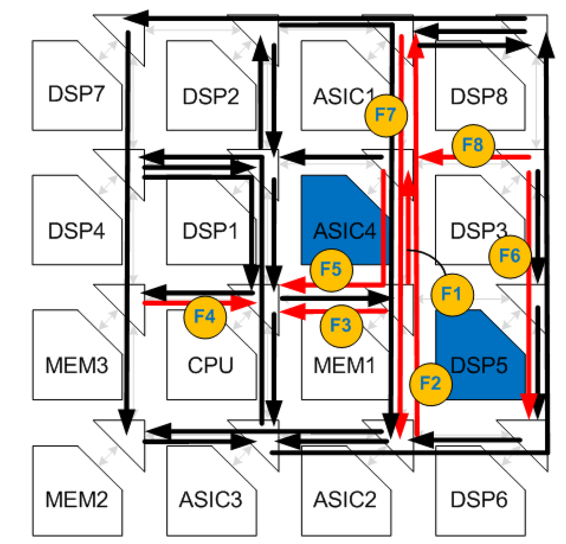




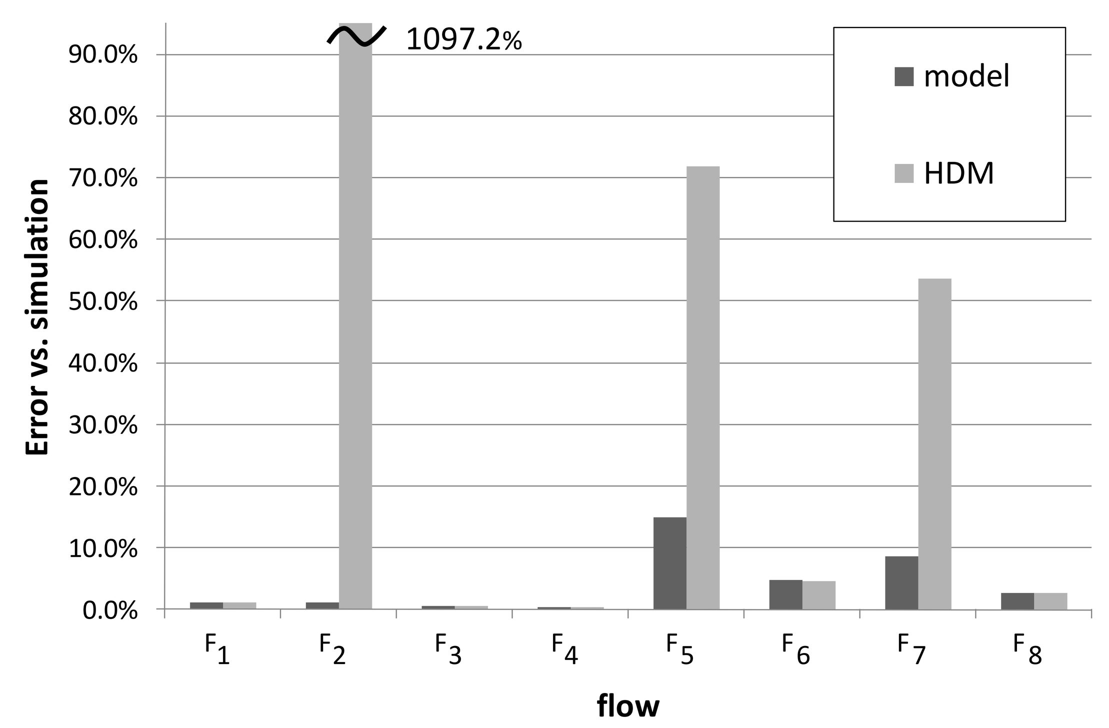


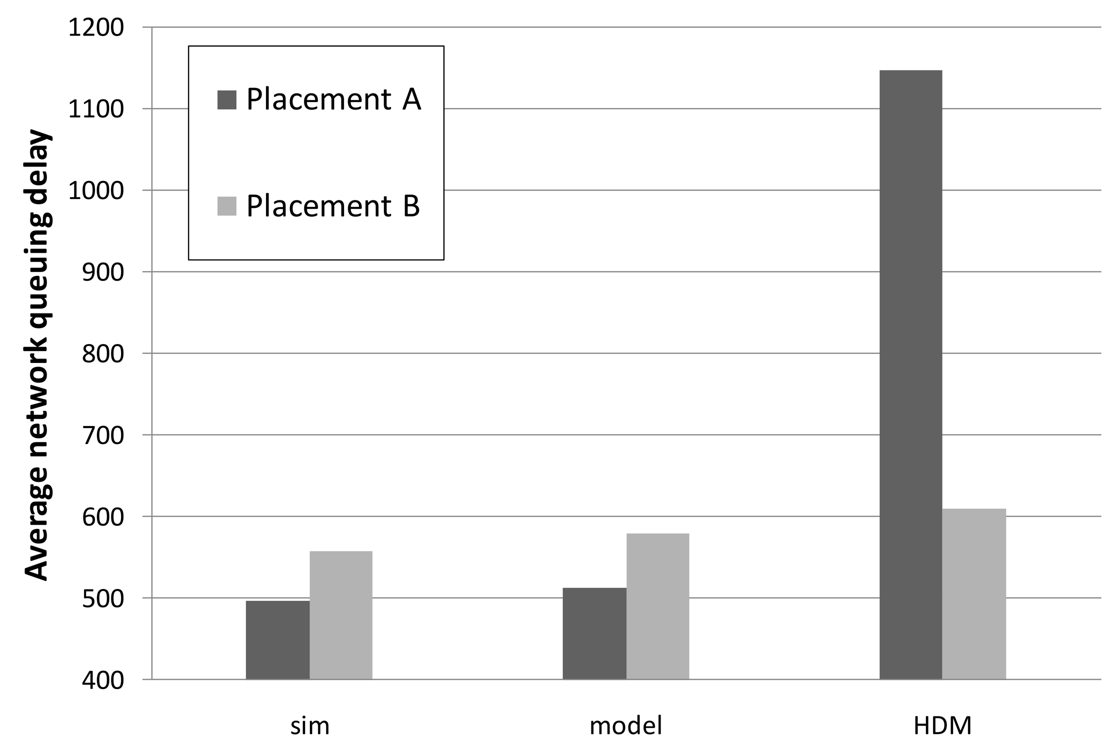


A possible use of the analytical delay model is to estimate network and flow properties within the inner-loop of a module placement optimization algorithm. Our model can quickly compute delay with high accuracy and we demonstrate that, contrary to HDM, it also reflects the change in delay as a result of varying module placement. Hence, our model can be used to predict, and correctly and efficiently choose between multiple placement options.



Placement A of the components and flows of the audio-video SoC. Placement B is achieved by swapping modules ASIC4 and DSP5





[1] A. Diamantidis and C. Papadopoulos. Exact analysis of a two-workstation one-buffer flow line with parallel unreliable machines. *European Journal of Operational Research, 2008.*
[2] Z. Guz, I. Walter, E. Bolotin, I. Cidon, R. Ginosar, and A. Kolodny. Network delays and link capacities in application-specific wormhole nocs. *Special Issue of the Journal of VLSI Design, 2007.*